REMARKS

Upon entry of the present amendment, none of currently pending claims 1-14 will have been amended and thus will remain pending in the present application. However, claims 20-24 will have been submitted for consideration by the Examiner. Accordingly, claims 1-14 and 20-24 are respectfully submitted for consideration and examination.

In view of the herein contained remarks, Applicants respectfully request reconsideration and withdrawal of each of the outstanding rejections together with an indication of the allowability of all of the claims pending in the present application, in due course. Such action is now believed to be appropriate and proper and is thus respectfully requested.

Initially, Applicants respectfully thank the Examiner for considering each of the documents cited in the Information Disclosure Statement filed on July 31, 2009 by the return of an appropriately annotated copy of the PTO 1449 form that was attached to the above noted Information Disclosure Statement.

In the outstanding official action, the Examiner rejected claim 1 under 35 USC 103(a) as being unpatentable over Sakuyama et al. (JP-06 061,636) in view of Applicants' admitted prior art ("AAPA"), or, in the alternative, as unpatentable over AAPA in view of Sakuyama et al. Claim 2 was rejected under 35 USC 103(a) as being unpatentable over Sakuyama et al. in view of AAPA or over AAPA in view of Sakuyama et al. and further in view of Crane et al. (U.S. Patent No. 6, 667, 194). Claims 3-5 were rejected under 35 USC 103(a) as being unpatentable over the combination applied against claim 2 and further in view of Nakamura et al. (U.S. Patent No. 6, 365, 499). Finally, claims 6-14 were rejected under 35 USC 103(a) as being obvious over Gonzalez et al.

(U.S. Patent Application Publication No. 2003/00804437) with supporting evidence of Hayama et al. (U.S. Patent No. 6, 051, 448).

Applicants respectfully traverse each of the above noted rejections and submit that they are inappropriate and improper with respect to the combinations of features recited in each of Applicant's claims. In particular, Applicants respectfully submit that none of the references of record in the present application, nor any proper combination of the references of record teach, disclose, suggest, or render obvious the present invention as defined by each of the particular combinations of features recited at least in Applicants' independent claims.

Applicants' invention is directed to an electronic component mounting method in which joints between a circuit substrate and electronic components are reinforced using a resin, as described in Applicants' independent claim 1. In particular, the method includes supplying an unhardened reinforcing resin on a circuit substrate and printing a solder paste on the reinforcing resin such that the reinforcing resin is disposed between the solder paste and bond areas of the circuit substrate. The electronic components, which have solder bumps, are placed on the circuit substrate and the reinforcing resin, the solder bumps, and the solder paste are heated such that the solder paste flows through the reinforcing resin and contacts the bond areas of the circuit substrate to interconnect the circuit substrate and the electronic components in response to heating of the reinforcing resin.

In particular, Applicants' claim requires, inter alia, printing a solder paste on the reinforcing resin. Neither of the two references applied against the claim 1, regardless of

the order or manner in which they are combined, teach, disclose or render obvious at least the above noted feature, in the claimed combination.

In this regard, Applicants note that the Examiner has asserted that Sakuyama et al. discloses separately applying resin and solder powder on a board substrate. However, even the Examiner does not assert that Sakuyama et al. discloses printing a solder paste on the reinforcing resin. Further, the Applicant admitted prior art (AAPA) of figure 10, to which the Examiner refers in the outstanding rejection, merely discloses printing of the solder paste onto the circuit substrate, not onto a reinforcing resin, as recited in Applicants' claim.

Additionally, the prior art of figure 10 of Applicants' application relates to a method that supplies the reinforcing material to the solder joints after the surface mount process steps (solder paste application, component placement, and solder bonding by reflow) have been performed and applying heat to harden the reinforcement material and to achieve the reinforcing effect for the joints. In this regard, the Examiner's attention is respectfully directed to paragraph [0012] of the corresponding published Patent Application No. 2007/0164079.

In direct contrast to the above, Sakuyama et al. discloses applying a resin and a solder powder onto the bond areas of the substrate. Accordingly, the melting process steps of the two prior art documents upon which the Examiner relies in combination are self-contradictory. The Examiner has set forth no proper logical reason for combining the disclosures of these references in the manner proposed in the outstanding rejection. Whether or not one or the other of the two relied upon references disclose solder bumps

on the components, the melting and mounting procedures utilized by each of these two references are mutually contradictory.

The Examiner indicated his appreciation that AAPA teaches the additional step of applying underfill resin 31 after solder bonding the components. However, the Examiner dismisses this feature by merely asserting that the rejection is not concerned with any subsequent step after bonding the components. However there is no basis for the Examiner to ignore portions of the disclosure of a reference that undermine the viability of the proposed combination without giving any logical or legal reason or basis for such action.

In setting forth the rejection, the Examiner asserts that the process of Sakuyama et al. in view of AAPA or the process of AAPA in view of Sakuyama is indistinguishable from the claimed process. This is clearly incorrect. As noted above, neither of two references discloses at least printing a solder paste onto a reinforcing resin.

Applicants note that in setting forth the rejection, the Examiner asserts that the process of Sakayama et al. in view of AAPA is indistinguishable from the claimed process, an assertion that has previously been shown to be inaccurate. Additionally, based on this assertion, the Examiner takes the position that it would necessarily flow that during the heating step, the solder paste would flow through the reinforcing resin and contact the bond areas on the substrate in order to interconnect the substrate and the electronic components. However, the Examiner has again provided no evidentiary support for his position.

In this regard, Applicants again submit that the Examiner is incorrect. In particular, AAPA teaches that the resin is supplied after setting of the solder paste.

Accordingly, it is clear that the paste cannot flow through the reinforcing resin and contact the bond areas. Additionally, the abstract Sakayama et al. contains no disclosure of this "necessarily" present feature.

Even further, the resin of Sakayama et al. is in fact an adhesive component of the solder paste. Thus, what Sakayama et al. teaches is independently applying two components of the paste onto the pads. This is rather remote from the disclosure of the AAPA that the Examiner attempts to combine with the disclosure of Sakayama et al.

In Sakayama, the resin is screen printed onto the pads and the solder, in powder form, and is subsequently sprayed onto the adhesive layer 3, thus forming a solder layer 4.

For each of the above noted reasons and certainly for all of the above noted reasons combined, it is respectfully submitted that claim 1 and those claims dependent thereon are clearly patentable over each proposed combination of references applied thereagainst. In this regard, Applicants note that the disclosures of Crane et al. and Nakamura et al. cannot supply the above noted deficiency of the combination of the two primary references. Nor has the Examiner even asserted that any of these secondary references provide teachings that would supply the above noted deficiency.

Accordingly, Applicants respectfully submit that claims 1-5 are clearly patentable over the references of record in the present application. An action to such effect is respectfully requested in due course.

A further aspect of Applicants' disclosed invention is reflected in the recitations of claim 6 which relates to an electronic component mounting method in which joints between a circuit substrate and electronic components are reinforced using a resin. In

particular, the method includes printing a solder paste on bond areas of the circuit substrate where electrodes of the electronic components are to be bonded then restricting fluidity of the solder paste so that the solder paste retains its shape as printed. A thermal settable reinforcing resin is then applied on the circuit substrate including the solder paste and electronic components, which have solder bumps, then are placed on the circuit substrate and the electronic components are then solder bonded on the circuit substrate and the reinforcing resin is hardened.

The above noted combination of features is not disclosed by Gonzalez et al. even when considered together with the supporting evidence of Hayama et al.

In setting forth the rejection applied to claim 6, the Examiner essentially takes the position that Gonzalez et al. teaches all of the claimed features and that Hayama et al. merely teaches that is known to print patterns of paste on a substrate. In discussing the disclosure of Gonzalez et al., the Examiner takes the position that the printed solder paste in the method of Gonzalez is restricted in fluidity since the deposited paste layer retains a given shape. However, this is not what Applicants' claim recites. In particular, Applicants' claim 6 recites first printing of a solder paste on bond areas of the circuit substrate and "then" restricting the fluidity of the solder paste. This is clearly not disclosed by Gonzalez et al.

In this regard, Applicants note that Gonzalez et al. merely discloses an ordinary re-flow process wherein the heat treatment is performed after joining of the components to the substrate. However, in the present invention, as recited in claim 6, restricting the fluidity of the solder paste is performed prior to the application of the reinforcing resin onto the circuit substrate. Additionally, Applicants' note that in Gonzalez et al., the

solder is optionally pre-coated and is already dried before the reflow process of Gonzalez et al. begins. Thus, it is clear and apparent that restricting the fluidity (i.e. drying) the solder is not at all inherent or even disclosed by Gonzalez et al.

Moreover, according to the teachings of the present invention, a solder paste is printed onto the bond areas of the circuit substrate. Gonzalez et al. also does not disclose the use of a solder paste but appears to relate to the use of a solder thin layer such as a foil. Accordingly, there are numerous significant and substantial differences between the disclosure of Gonzalez et al. and the electronic component mounting method recited in Applicants' claim 6.

Accordingly, for each of the above noted reasons individually and even more certainly in view of all of the above noted reasons taken in combination, claim 6 and those claims dependent thereon are submitted to be clearly patentable over the prior art of record in the present application. An action to such effect is respectfully requested.

By the present response, Applicants have submitted a number of additional claims for consideration by the Examiner. Each of these claims is submitted to be patentable over the references of record in the present application, at least based upon their particular recitations. In particular, none of the references disclose the adhesive powers of the resin sheet sides as recited, in the claimed combination. Accordingly, examination and an indication of the allowability of the newly submitted claims are respectfully requested.

SUMMARY AND CONCLUSION

By the present response, Applicants submit that they have made a sincere effort to place the present application in condition for allowance and believe that they have now done so. Applicants have not amended any of the pending claims but have rather submitted several additional claims for consideration by the Examiner.

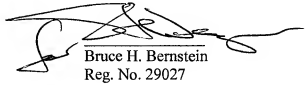
Applicants have discussed the disclosures of the references and pointed out the shortcomings thereof. In particular, Applicants have discussed the features of the present invention and have pointed out the deficiencies of the disclosures of the reference with respect thereto. Further, Applicants have discussed the explicit recitations of the pending claims and have contrasted the same with the disclosures of the references, both individually as well as in any proper combination. Applicants have further pointed out the lack of a logical reason for the combinations proposed by the Examiner. Applicants have also provided a basis for the allowability of the newly submitted claims.

Accordingly, Applicants have provided a clear and convincing evidentiary basis supporting the patentability of all the claims in the present application and respectfully request indication to such effect, in due course.

Should any fees be necessary to maintain the pendency of this application, including any extensions of time required to place the application in condition for allowance by an Examiner's Amendment, the Commissioner is hereby authorized to charge any additional fee to Deposit Account No. 19-0089.

Should the Examiner have any questions or comments regarding this Response, or the present application, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully Submitted,
Hirokazu Maeda



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